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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,397	12/12/2003	Wee-Kuan Gan	4413-0132P	9139

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,397	GAN ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/9/2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4 and 5 is/are rejected.

7)☒ Claim(s) 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 as amended on 5/9/2006 are pending in the instant application. Applicant's arguments and amendments have been fully and carefully considered and are partially persuasive. However, the 102(b) rejection of claims 1, 2, 4, and 5 is maintained. Accordingly, this action is made **FINAL**.

Specification

2. The amendments to the specification, as discussed in Applicant's remarks on page 10 paragraphs 2-5, are sufficient to overcome the Examiner's objection to the specification. Accordingly, the objection to the specification is withdrawn.

Claim Objections

3. The amendment to claim 1 regarding the Examiner's objection to claim 1, as discusses in Applicant's remarks on page 10 paragraph 6, is sufficient to overcome the Examiner's objection to claim 1. Accordingly, the Examiner's objection to claim 1 is withdrawn.

4. **Claim 3** is objected to because of the following informalities: Claim 3 recites the limitation "*said check area in said page of child block* " in line 3. Claim 1 refers to "*a page of said child block*" into which data is recorded and "*a redundant page, which stores metadata in said child block*". In the interest of maintaining clear, consistent terminology, the Examiner suggests amending "*said check area in said page of child*

block " to read "said check area in said redundant page of child block ". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The amendments to claims 1-5, as discussed in applicant's remarks on page 11 paragraphs 1-3, are sufficient to overcome the rejection of these claims under 35 USC 112 second paragraph. Accordingly, the rejection of claims 1-5 under 35 USC 112 second paragraph is withdrawn.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1,2,4, and 5** are rejected under 35 U.S.C. 102(b) as being anticipated by Pua et al (US 2002/0147882).

8. **Claim 1** is taught by Pua as:

a. *A linking method under a mother and child block architecture for building a check area and a logical page of a child block in a flash memory, wherein when a host writes data into a logical block of said flash memory.* See paragraph 0002, which shows that the current invention is directed to a flash memory device.

b. *The linking method comprising: defining a block corresponding to said logical block as a mother block.* The mother block is defined as the block corresponding to the logical address received from the host in paragraph 0118.

c. *Locating a new block from a backup block and defining said new block as a child block.* See paragraph 0121, which shows that a clean block is taken from the FIFO to create a child block.

d. *Wherein said mother block and said child block have the same logical address.* See paragraph 0033, which shows that the mother block and the child block have the same logical address.

e. *Recording the data into a page of said child block, while retaining original data in said mother block.* See paragraph 0124, which discusses step 608 of figure 6, in which the data is written to the child block. Paragraph 0127 shows that the mother block is not erased until all the data of the mother block is written to the child block. Accordingly, the data is recorded into a page of the child block and retained in the mother block until all pages of the mother block are copied.

f. *Using a redundant page, which stores metadata in said child block for creating a check area.* Paragraph 0030 shows that at initialization of the flash memory, all the blocks are searched to determine the relationship between the physical blocks in the flash memory and the logical blocks of the stored data. In order to do this, it is inherent that each block has an area that stores the logical block identifier for the data stored in that physical page. These identifiers form the link table that maps the logical addresses to physical addresses.

g. *Recording said redundant page of said child block which corresponds to a page in said mother block.* Paragraph 0033 shows that the logical address corresponding to the mother block is mapped to refer to the child block. In order for the memory to be initialized as taught by paragraph 0030, the logical address corresponding to the child block must be recorded in the child block.

h. *And using said check area consisting of a logical page for identifying whether the data to be retrieved is stored in said mother block or child block when a subsequent read is performed.* As shown in paragraph 0030, at initialization the link table is read from each of the physical blocks of the flash memory. This link table associates a physical block with the corresponding logical block so the system can identify if that logical block should be read from the child physical block or the mother physical block.

9. **Claim 2** is taught by Pua as:

i. *Wherein when a host is ready for reading said page in said logical page, said child block corresponding to said mother block in said logical page is read and other pages in said child block are read all from said pages of said mother block.* Paragraph 0132 shows that when a read is performed, the logical address sent from the host is converted into the physical address of the block and page. The data is then read from this location, which is the child block.

10. **Claim 4** is taught by Pua as:

j. *Wherein when said host repeats writing data into said logical page of the child block, the data being written to a full page of said child block and when said*

logical page of child block is full, a new block is located for moving a valid block of said mother block and said child block into therein and then said mother block and child block are erased. In the invention disclosed by Pua, when a write is made to a page that has been written to previously in the child page, a new child is selected in the same manner shown in paragraphs 0118-0130. When a child block is chosen, the mother block is moved into the FIFO queue where it becomes an available block.

11. **Claim 5** is taught by Pua as:

k. *A linking method under a mother and a child block architecture for building a check area and a logical page of a child block in a flash memory, wherein when a host writes data into a logical block of said flash memory, the writing method comprising*: See paragraph 0002, which shows that the current invention is directed to a flash memory device.

l. (a) *Defining an actual page corresponding to a logical page as a mother block.* The mother block is defined as the block corresponding to the logical address received from the host in paragraph 0118.

m. (b) *Locating a new block and defining it as a child block.* See paragraph 0121, which shows that a clean block is taken from the FIFO to create a child block.

n. (c) *Writing data into said logical page of said child block while retaining original data in said mother block.* See paragraph 0124, which discusses step 608 of figure 6, in which the data is written to the child block. Paragraph 0127

shows that the mother block is not erased until all the data of the mother block is written to the child block. Accordingly, the data is recorded into a page of the child block and retained in the mother block until all pages of the mother block are copied.

o. (d) *Marking a check area of said redundant page in said child block belonging to a page of said mother block.* Paragraph 0033 shows that the logical address corresponding to the mother block is mapped to refer to the child block. In order for the memory to be initialized as taught by paragraph 0030, the logical address corresponding to the child block must be recorded in the child block.

Allowable Subject Matter

12. **Claim 3** is objected to as being dependent upon a rejected base claim and containing a minor informality, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and correcting the informality discussed *supra*.

13. **Claim 3** recites the limitation "*wherein said check area in said page of child block is defined as three bytes, wherein a first and second byte indicate pages of said child block and a third byte indicates a page of said mother block.*" This limitation is not taught or suggested by the prior art of record.

Response to Arguments

14. Applicant's arguments submitted 5/9/2006 have been carefully and fully considered, but are only partially persuasive.

15. Applicant's amendments and remarks regarding the Examiner's objection to the specification, see page 10 paragraphs 2-5, are sufficient to overcome the Examiner's objection to the specification.

16. Applicant's amendment and remarks regarding the Examiner's objection to claim 1, see page 10 paragraph 5, are sufficient to overcome the Examiner's objection to claim 1.

17. Applicant's amendments and remarks regarding the rejection of claims 1-5 under 35 USC 112 second paragraph, see page 11 paragraphs 1-3, are sufficient to overcome the rejection of said claims under 35 USC 112 second paragraph.

18. Applicant states at page 11 paragraph 4, "*In view of the above amendments and remarks, it is believed that the claims clearly distinguish over the patent relied upon by the Examiner.*" The Examiner respectfully disagrees, and refers Applicant to the rejection of claims 1, 2, 4, and 5 *supra*.

19. Applicant's remarks regarding the prior art cited by the examiner, see page 12 paragraph 1, are not fully understood by the Examiner. Applicant states at page 12 lines 1-3 "*Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.*" The Examiner respectfully submits that the only prior art cited was the US Patent

Application Publication US 2002/0147882 to Pua et al., which relied upon in the rejection of claims 1, 2, 4, and 5 under 35 USC 102 (b).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian R. Peugh
Primary Examiner

Jared I Rutz
Examiner
Art Unit 2187

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